Digitally Controlled Rectifier for Wireless Power Receivers

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***Abstract*—Reducing power loss in wireless power receivers is important to avoid thermal design issues. Synchronous rectification is a suitable means for loss reduction. In this paper we propose a synchronous rectifier with a simple control scheme. A detailed analysis leads to a time-domain model which is used to perform a power loss analysis. Experimental verification shows that the predicted efficiency improvement agrees with measurement results.**

***Index Terms*—Wireless power transmission, efficiency, synchronous rectifier**

I. Introduction

Thanks to the advent in power electronics, more and more devices use wireless power transmission (WPT) for power or battery charging. Among the many benefits, it was recognized by a group of leading industrial companies that WPT has the potential of unifying the charging of mobile devices. This resulted in the foundation of the Wireless Power Consortium (WPC) and publication of the first international standard for providing up to 5W of power to phones, cameras and batteries in the year 2010 [1]. The consortium has defined the Qi logo which indicates that a device is compatible to the WPC standard and complies with its requirements on interoperability and performance.

Despite the advances that have been made over the past years, reduction of power losses is still a design challenge. In highly integrated and small mobile devices power loss is one of the most critical design constraints as the power loss generates heat. This is particularly an issue for temperature sensitive LiIon batteries and could introduce component thermal stress.

A major part of the power loss is caused by the forward voltage drop of the rectifier diodes in the power receiver (Rx). In many cases passive full-bridge rectifiers are used. Despite its simplicity the drawback of this rectifier is that there are always two diodes conducting at the same time which results in higher power loss. This is particularly an issue for low output voltage WPT systems. For example, the efficiency of a WPT system with 5V output voltage drops by 15% when a Schottky bridge rectifier, with a typical voltage drop of $2 \times 0.45V$, is used.

The forward voltage drop issue can be resolved using synchronous rectification. Typically the timing of the synchronous rectifier is optimized to maximize the conduction time of the MOSFETS. This requires a high speed and complex control and drive circuit which also consumes power [2]. Other implementations work well under normal conditions but show serious issues during power-up and down [3].

In this paper we propose a simple and cost-effective synchronous full-bridge rectifier. We will describe later that the control of the synchronous rectifier does not depend on current measurements and that exact timing of the switching instants is not necessary. This results in a simple control scheme that can be implemented on almost any commercially available low-cost MCU, which is already available in most wireless power receivers for monitoring and control purposes. By making use of digital control, proper power-up and down can be guaranteed.

II. Qi-Compliant WPT System

A Qi-compliant WPT system that corresponds to the A1 transmitter design as defined in the WPC standard [4] is depicted in Fig. 1. A half-bridge inverter which consists of MOSFETs $M1_T$ and $M2_T$ drives the Tx resonant circuit. The resonant circuit comprises the Tx coil L_T and resonant capacitor C_T. The Rx coil is inductively coupled to the Tx coil in order to enable power transfer. Capacitor C_R is used to match the load network to the output impedance of the inductive link to enhance the power transfer efficiency. According to the WPC standard a parallel capacitor C_d is required to enable resonant detection of the power receiver. Furthermore a load modulator circuit is required to transmit data to the power transmitter. Fig. 1 shows a capacitive load modulator which consists of the capacitors C_{m1} and C_{m2} as well as the modulator switches $M5$ and $M6$. If the modulator switches are turned on the series connection of C_{m1} and C_{m2} is parallel to C_d. The effective parallel capacitance significantly influences the operation of the rectifier and needs to be considered in the subsequent analysis. In this figure the load is connected to the resonant circuit through a passive full-bridge rectifier.

III. Synchronous Rectifier

Fig. 2 shows a simplified schematic of the proposed synchronous rectifier (SR). The secondary coil and resonant capacitor are modeled as a current source. The parallel capacitor C represents the equivalent capacitance of C_d, C_{m1} and C_{m2}. MOSFETs $M3$ and $M4$ are cross-connected and replace the low side diodes in the passive bridge rectifier. The semi-active rectifier which comprises $M3$ and $M4$ is self-driven as the gate voltages are equal to the rectifier input voltage. The rectifier input voltage has an approximately rectangular waveshape when the output voltage is nearly constant.

Adaption of this self-controlled driving scheme to all four MOSFETs as in [3] causes significant issues during start-up and power-down of the circuit. To solve these issues the

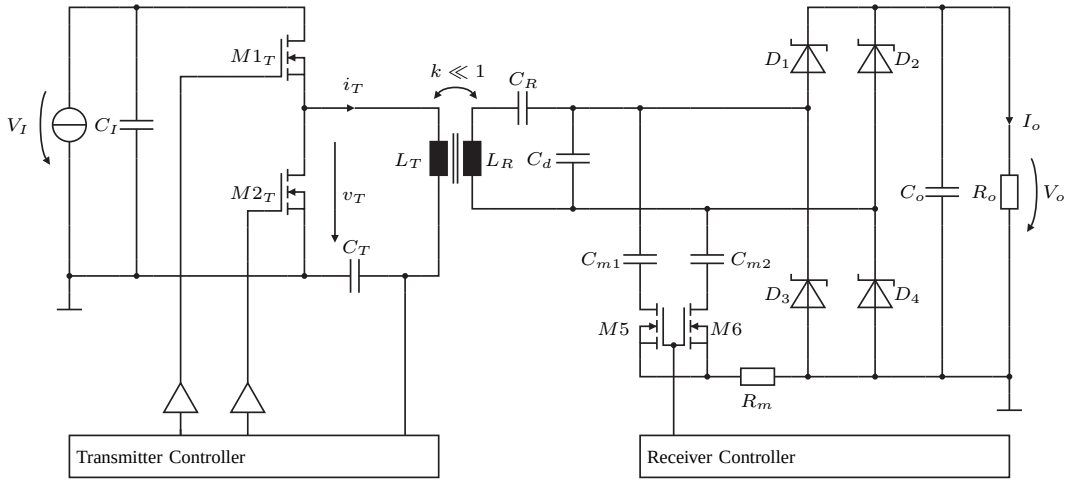

Figure 1. Qi-compliant WPT circuit using an A1 transmitter design as specified in the WPC standard [4]

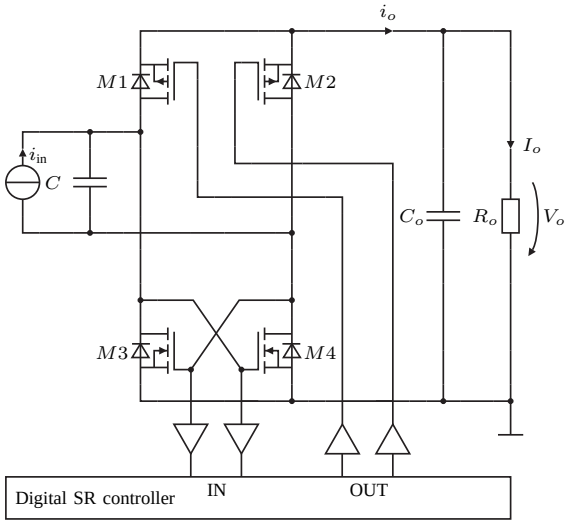

Figure 2. Proposed synchronous full-bridge rectifier

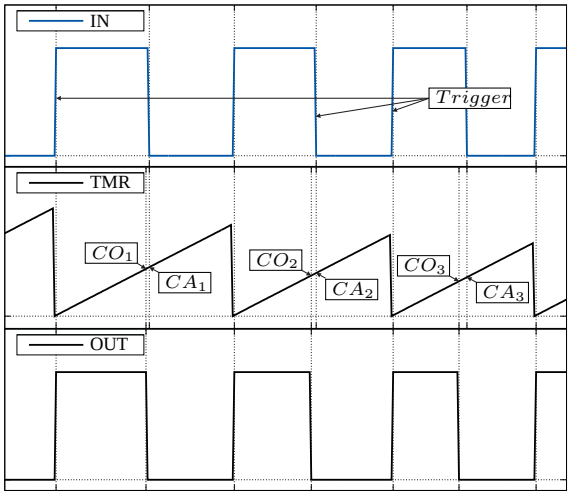

Figure 3. Input and output signal at the MCU with corresponding timer. The second timer works similar, but with an phase shift of one half period.

drive signals of the upper MOSFETs are generated by the digital SR controller in Fig. 2 which can be implemented on a standard MCU. The IN-signal of the digital SR controller is directly derived from the gate drive signals of $M3$ and $M4$. Referring to Fig. 3 a rising edge of an IN-signal resets a timer and toggles the corresponding OUT-signal into high state which, in fact, turns-on one of the upper MOSFET ($M1$ or $M2$). The OUT-signal goes low when the counter value equals the compare value CO_n which was determined at the time instant of the falling edge of the IN-signal in the previous cycle CA_{n-1}.

For proper operation of the circuit it is essential to maintain the self-driven operation of $M3$ and $M4$ which requires natural commutation of the current in the rectifier. This is achieved by turning off both of the upper MOSFETs before the end of the cycle which requires that $CO_n < CA_{n-1}$. In a practical implementation CO_n will be calculated based on the turn-off delay time plus an additional delay time as a design margin. The additional delay leads to increased power loss as the current flows through the body diode during that time. However, as illustrated in Fig. 4, the current at the end of the half-period is already close to zero and the additional loss is small. The proposed rectifier has, therefore, slightly higher conduction losses compared to more complex control schemes but a much simpler and efficient control circuit.

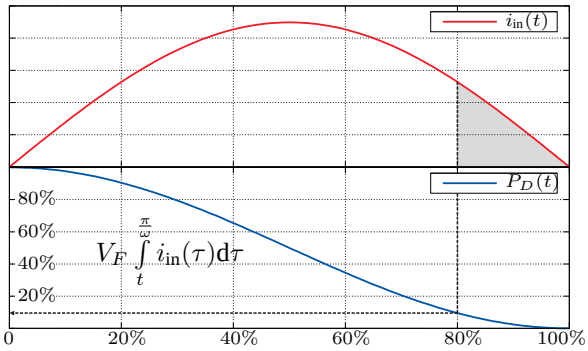

Figure 4. Diode losses

IV. Circuit Analysis

In the subsequent sections we assume that

1) the output voltage of the wireless power receiver is constant which implies that the output voltage ripple is not considered
2) the current through the secondary coil winding $i_{\text{in}}(t)$ is purely sinusoidal and is described by $i_{\text{in}}(t) = \hat{I}_{\text{in}} \sin(\omega t)$, an approximation that is well fulfilled in WPT systems operating close to the resonance frequency [5]
3) the circuit operates in the periodical steady-state which implies that any waveform can be described in the form $x(t) = x(t+T)$, where T is the period length

The circuit analysis is carried out for the first half-period of the secondary coil current. The analysis of the second half-period can be performed in a similar way and yields basically identical results.

A. Interval 1 ($t_0 < t \leq t_{on}$)

Depending on the capacitor voltage at the time instant when $M1$ turns on the first interval consists of either one or two subintervals.

Subinterval 1a ($v_C(t_{on}) < V_o + V_F$): This case is illustrated in Fig. 5. At $t = t_0 = 0$ the instantaneous voltage across C is $v_C(t_0)$ and the sinusoidal current out of the resonant tank starts to charge C towards positive values. $M1$ and $M2$ are turned-off and their body diodes are blocking because the output voltage is higher than the voltage across C in this time interval. The voltage across the capacitor can be calculated by integration of the current, starting at the voltage $v_C(t_0)$

$$v_C(t) \;=\; v_C(t_0) + \frac{1}{C}\int_{t_0}^{t} i_{\text{in}}(\tau)\mathrm{d}\tau \tag{1}$$

As mentioned above, both high side diodes are in blocking state and the complete resonant current charges the capacitor C. The current flowing towards the output equals zero. At the end of Subinterval 1a the instantaneous capacitor voltage is lower than the output voltage. When MOSFET $M1$ is turned on the voltage difference $v_C(t_{\text{on}}) - V_o$ causes a large negative current pulse that quickly charges the capacitor. The amplitude of this pulse is only limited by $R_{DSn} + R_{DSp}$. The resulting power loss is significant and, therefore, this operation mode should be avoided for high efficiency.

Subinterval 1b ($v_C(t_{on}) \geq V_o + V_F$): The aforementioned losses practically disappear if MOSFET $M1$ is turned on when the capacitor charged to or slightly above $V_o + V_F$. This case is illustrated in Fig. 6. At the time instant t_1 the capacitor voltage (1) equals $V_o + V_F$ and the body diode of $M1$ is conducting current in forward direction. R_{DSn} represents the drain-to-source resistance of $M4$. Applying Kirchhoffs node and mesh equations yields

$$R_{DSn} C \frac{v_C(t)}{dt} + v_C(t) = V_o + V_F + R_{DSn} i_{\text{in}}(t) \tag{2}$$

The solution of this linear differential equation can be found in many textbooks, e.g. [6]. With $v_C(t_1) = V_o + V_F$ we get

$$v_C(t) = V_o + V_F + \ldots \\ \ldots + \frac{R_{DSn}\hat{I}_{\text{in}}}{1 + \left(\dfrac{\omega}{\lambda_{1b}}\right)^2} \cdot \left\{ a_{1b}(t) - b_{1b}\, e^{\lambda_{1b}(t-t_1)} \right\} \tag{3}$$

where $\lambda_{1b} = -1/R_{DSn}C$ and

$$a_{1b}(t) = \frac{\omega}{\lambda_{1b}} \cos(\omega t) + \sin(\omega t) \tag{4}$$

$$b_{1b} = \frac{\omega}{\lambda_{1b}} \cos(\omega t_1) + \sin(\omega t_1) \tag{5}$$

The current flowing towards the output is

$$i_o(t) \;=\; \frac{v_C(t) - V_o - V_F}{R_{DSn}}. \tag{6}$$

B. Interval 2 ($t_{on} < t \leq t_{off}$)

At t_{on} MOSFET $M1$ is turned on. Note that, depending on the previous interval the current pulse at this time instant is negative and large (subinterval 1a) or positive and small (subinterval 1b). Turning on $M1$ at the end of subinterval 1b is therefore the preferred operating mode. In interval 2 the capacitor is connected to the output voltage source through the resistors R_{DSn} and R_{DSp} as shown in Fig. 5. R_{DSn} represents the drain-to-source resistance of $M4$ and R_{DSp} is the drain-to-source resistance of $M1$. Applying Kirchhoffs node and mesh equations yields

$$R_{DS} C \frac{\mathrm{d}v_C(t)}{\mathrm{d}t} + v_C(t) = V_o + R_{DS}\, i_{\text{in}}(t) \tag{7}$$

where $R_{DS} = R_{DSn} + R_{DSp}$. The solution of this linear differential equation is

$$v_C(t) = V_o - (V_o - v_C(t_{\text{on}}))\, e^{\lambda_2 (t - t_{\text{on}})} + \ldots \\ \ldots + \frac{R_{DS}\hat{I}_{\text{in}}}{1 + \left(\dfrac{\omega}{\lambda_2}\right)^2} \cdot \left\{ a_2(t) - b_2\, e^{\lambda_2 (t - t_{\text{on}})} \right\} \tag{8}$$

where $\lambda_2 = -1/R_{DS}C$ and

$$a_2(t) = \frac{\omega}{\lambda_2} \cos(\omega t) + \sin(\omega t) \tag{9}$$

$$b_2 = \frac{\omega}{\lambda_2} \cos(\omega t_{\text{on}}) + \sin(\omega t_{\text{on}}) \tag{10}$$

During this time interval the output current can then be calculated from

$$i_o(t) \;=\; \frac{v_C(t) - V_o}{R_{DS}} \tag{11}$$

C. Interval 3 ($t_{off} < t \leq t_2$)

Turning off $M1$ at $t = t_{\text{off}}$ leads to the condition, that $v_C(t_{\text{off}})$ is smaller than the voltage that is necessary to drive a current through the diodes. The parasitic diodes of

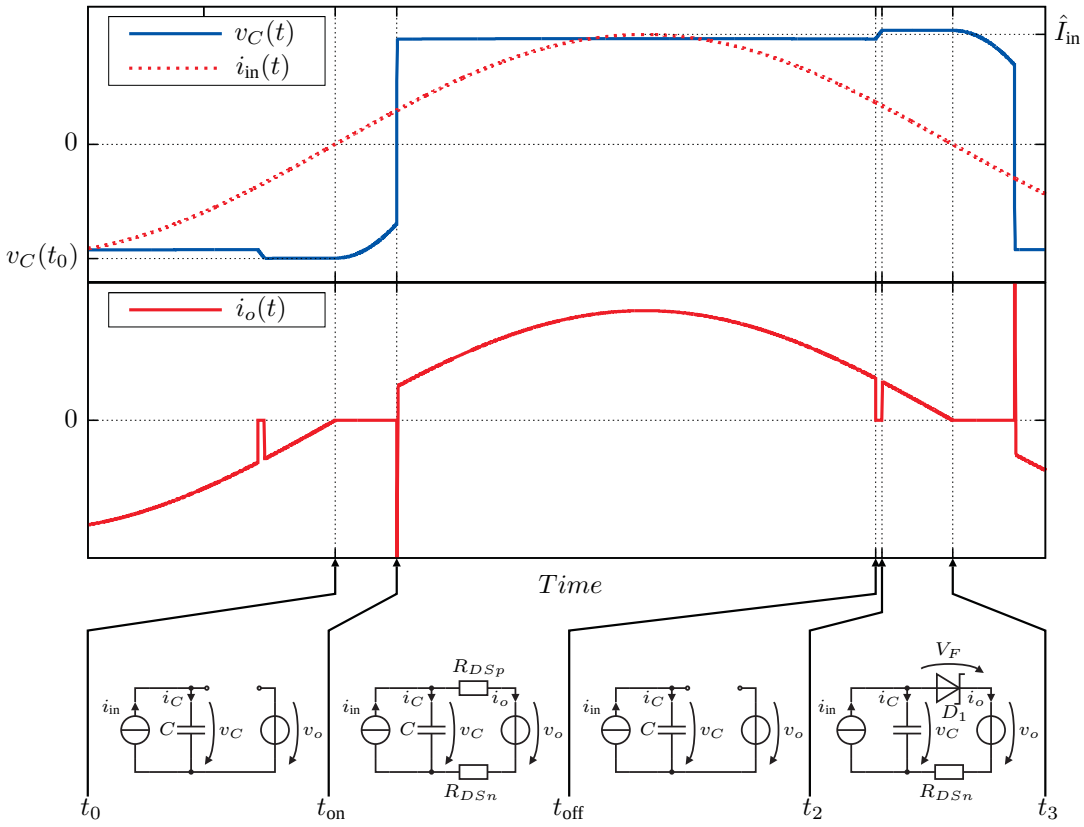

Figure 5. One half period of the rectifier input voltage $v_C(t)$ and the output current $i_o(t)$ at sinusoidal input current $i_{\text{in}}(t)$.

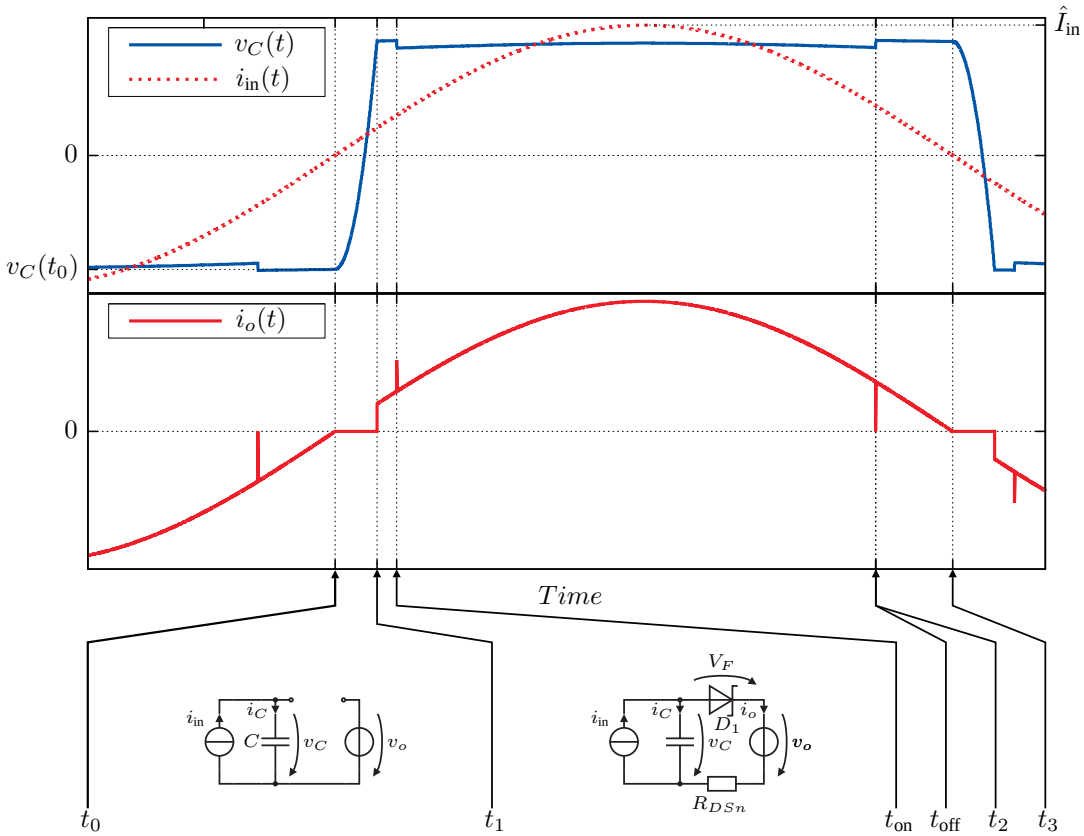

Figure 6. One half period of the rectifier input voltage $v_C(t)$ and the output current $i_o(t)$ at sinusoidal input current $i_{\text{in}}(t)$.

both, $M1$ and $M2$ are blocking and the voltage across C is

$$v_C(t) \;=\; v_C(t_{\text{off}}) + \frac{1}{C}\int\limits_{t_{\text{off}}}^{t} i_{\text{in}}(t)\mathrm{d}t \tag{12}$$

The current flowing towards the output during interval 3 equals zero.

D. Interval 4 ($t_2 < t \leq t_3$)

In the forth time interval we have conditions similar to subinterval 1b. The capacitor voltage can again be derived from (2). With $v_C(t_2) = V_o + V_F$ the solution of this linear differential equation is

$$\begin{aligned} v_C(t) &= V_o + V_F + \ldots \\ &\quad \ldots + \frac{R_{DSn}\hat{I}_{\text{in}}}{1+\left(\dfrac{\omega}{\lambda_4}\right)^2} \cdot \left\{ a_4(t) - b_4\, e^{\lambda_4 (t-t_2)} \right\} \end{aligned} \tag{13}$$

where $\lambda_4 = -1/R_{DSn}C$ and

$$a_4(t) = \frac{\omega}{\lambda_4}\cos(\omega t) + \sin(\omega t) \tag{14}$$

$$b_4 = \frac{\omega}{\lambda_4}\cos(\omega t_2) + \sin(\omega t_2) \tag{15}$$

The current flowing towards the output is given by (6).

E. Time-Domain Model and Numerical Solution

The capacitor voltage during the first half-period is

$$v_C(t) \;=\; \begin{cases} (1) & \text{if} \quad t_0 < t \leq \min(t_1,\, t_{\text{on}}) \\ (3) & \text{if} \quad \min(t_1,\, t_{\text{on}}) < t \leq t_{\text{on}} \\ (8) & \text{if} \quad t_{\text{on}} < t \leq t_{\text{off}} \\ (12) & \text{if} \quad t_{\text{off}} < t \leq t_2 \\ (13) & \text{if} \quad t_2 < t \leq t_3 \end{cases} \tag{16}$$

while the current delivered to the load is given by

$$i_o(t) \;=\; \begin{cases} (6) & \text{if} \quad \min(t_1,\, t_{\text{on}}) < t \leq t_{\text{on}} \\ & \text{or} \quad t_2 < t \leq t_3 \\ (11) & \text{if} \quad t_1 < t \leq t_2 \\ 0A & \text{otherwise} \end{cases} \tag{17}$$

Independent parameters in these equations are the switching time instants t_0, t_{on}, t_{off} and the DC load current I_o. In order to calculate the voltage and current waveforms using (16) and (17) the four dependent parameters $v_C(t_0)$, t_1, t_2 and $\hat{I}_{\text{in}}$ need to be known. Time instant t_1 is only required if subinterval 1b exists, which is the case for $v_C(t_{\text{on}}) \geq V_o + V_F$. The dependent parameters can be determined numerically by solving the following conditions:

1) The circuit is in periodical steady-state and both half-periods are symmetrical. With $t_3 = t_0 + T$ we have
$$v_C(t_0) = -v_C(t_0 + T) \tag{18}$$
2) The average of $i_o(t)$ over the half-cycle must be equal to the DC load current I_o
$$\frac{\omega}{\pi}\int\limits_{0}^{\pi/\omega} i_o(t)\mathrm{d}t \;=\; I_o. \tag{19}$$
3) $v_C(t_2) = V_o + V_F$.
4) If $v_C(t_{\text{on}}) \geq V_o + V_F$ the following condition has to be evaluated to find t_1
$$v_C(t_1) = V_o + V_F \tag{20}$$

We have now a complete time-domain model of the proposed synchronous rectifier. It can be solved numerically to obtain the capacitor voltage and output current waveforms required for efficiency calculations.

F. Power Loss Analysis

Gate drive of the lower MOSFETs is lossless whereas the gate drive losses for the upper MOSFETs are

$$P_d \;=\; Q_G V_o \frac{\omega}{\pi}. \tag{21}$$

Switching losses

$$\begin{aligned} P_{sw} \;=\; \frac{\omega}{6\pi}\Bigg[&\frac{(v_C(t_{\text{on}}) - V_o)^2}{R_{DS}} t_r + \ldots \\ &\ldots + \frac{(v_C(t_{\text{off}}) - V_o)^2}{R_{DS}} t_f \Bigg] \end{aligned} \tag{22}$$

Conduction losses

$$P_c \;=\; \frac{\omega}{\pi}\int\limits_{0}^{\pi/\omega} (v_C(t) - V_o)\, i_o(t)\mathrm{d}t \tag{23}$$

Total rectification loss

$$P \;=\; P_d + P_{sw} + P_c \tag{24}$$

V. Model Verification

The model is verified experimentally using a Qi compliant WPT system including a prototype of the synchronous rectifier. The SR controller is implemented using two timers of a STM8L151G4 8-bit MCU running at 16MHz clock frequency [7]. The following model parameters were used: operating frequency $f = 1/T = 150\,\text{kHz}$, n-channel MOSFETs $M3$, $M4$ are FDS9926A ($R_{DSn} = 30\,\text{m}\Omega$, $Q_g = 6.2\,\text{nC}$, $t_r = 9\,\text{ns}$, $t_f = 15\,\text{ns}$, $V_F = 0.7\,\text{V}$), p-channel MOSFETS $M1$, $M2$ are FDS6875 ($R_{DSp} = 30\,\text{m}\Omega$, $Q_g = 23\,\text{nC}$, $t_r = 15\,\text{ns}$, $t_f = 35\,\text{ns}$, $V_F = 0.7\,\text{V}$), $CO_n = CA_{n-1} - 10$ and $t_{\text{on}} - t_0 = 300\,\text{ns}$.

According to the WPT standard data transmission to the transmitter can be implemented using capacitive load modulation as shown in Fig. 1. The influence of the modulation on the power loss is considered as follows: We have $C = 13\,\text{nF}$ when the the modulator switches (C_{m1} and C_{m2} in Fig. 1) are closed and $C = 2\,\text{nF}$ otherwise. The modulator switches are turned on for about 20% of the period length. The average power loss is $P_{av} = 0.2 \times P_{modulated} + 0.8 \times P_{unmodulated}$ which is used to predict the efficiency improvement in Fig. 7. The efficiency improvement due to the SR rectifier is shown relative to the efficiency of the same WPT system with passive rectification using the body diodes of the MOSFETs. Also shown in the figure are results for the

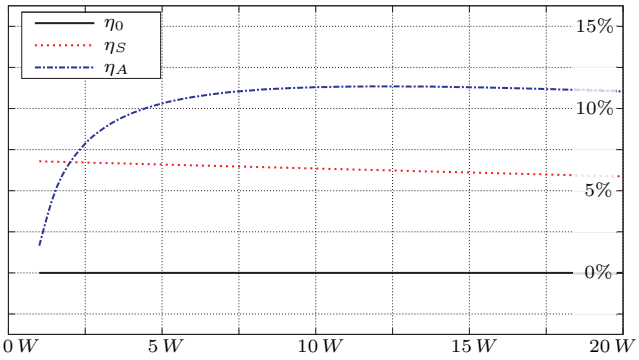

Figure 7. Efficiency Improvement normalized to η_0 which is the efficiency with a passive rectifier. η_S is the efficiency with a semi-active rectifier (lower MOSFETs are self-driven and only the body diodes of the upper MOSFETs are active) and η_A is the efficiency with the proposed full-synchronous rectifier

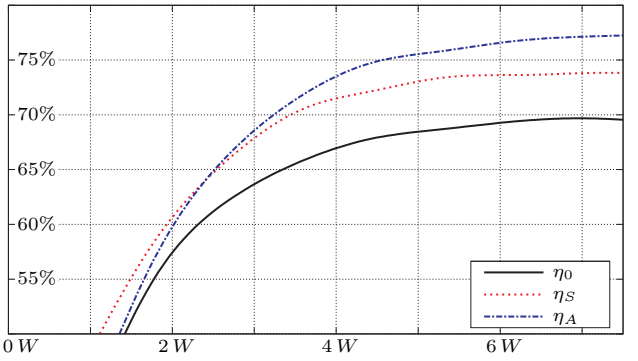

Figure 8. Efficiency measurements. η_0 is the efficiency with a passive rectifier. η_S is the efficiency with a semi-active rectifier (lower MOSFETs are self-driven and only the body diodes of the upper MOSFETs are active) and η_A is the efficiency with the proposed full-synchronous rectifier

semi-active rectifier where the lower MOSFETs are self-driven and the body diodes of the upper MOSFETSs are used.

The predicted efficiency improvement (Fig. 7) and measured efficiency in Fig. 8 are in good agreement. The efficiency curves drop off at low output power due to the quiescent power consumption of the system. The prediction of the crossing points is very accurate. The measured efficiency improvement is slightly lower than predicted. The reason for this is that not all dissipative circuit elements, such as the ESR of the output bulk and resonance capacitors, have been included in the model. If necessary the ESR values can be added to R_{DSn} and R_{DSp}.

VI. Discussion

We have already discussed that turning on the upper MOSFETs during subinterval 1a causes a large current to charge C and results in a low efficiency. With a fixed load t_{on} can be adjusted to guarentee turn-on in subinterval 1b (Fig. 5). Reducing the load leads to a smaller i_{in} and, therefore, the voltage increase across C is slowing down. With a fixed t_{on} the upper MOSFETs will turn on in subinterval 1a if the load gets small enough as illustrated in Fig. 6. This effect can also be seen in Fig. 8 as a rapid efficiency drop when the load is reduced. In the figure the efficiency curve of the proposed SR crosses the curve for the semi-active rectifier at approximately 2.5 W. Below this output power the rectifier should be operated in semi-active mode.

Similary, if the load is constant an increase of the capacitance C also increases the charging time and the upper MOSFETs may turn on too early. This could for example happen every time the modulator switch is closed. Therefore, operation of the SR in semi-active mode when the modulation switches are turned on could be benefitial. Ideally a look-up table which contains t_{on} for a set of load ranges is used to optimize t_{on}. Different data sets could be used depending on the modulator state.

VII. Conclusions

We have proposed a synchronous rectifier with a simple control scheme and demonstrated that an implementation on an off-the-shelf and low-cost microcontroller is feasible. A prediction of the efficiency improvement was made based on a detailed circuit and loss analysis. Efficiency measurements on an experimental setup have been carried out to show that the predicted efficiency improvements are sufficiently accurate. Thanks to digital control the rectifier works properly during start-up, power-down and load changes. Future work should include an adaptive adjustment of t_{on} and t_{off} to further maximize efficiency independent of parameter variations.

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